SystemVerilog for Design

Sandeepani is a training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for Xilinx in India for past 20 years

Start date: 21-Dec-2020 to 23-Dec-2020 (10.30am to 1.30pm)

Course Description:
This course explains how to write SystemVerilog models at the Register Transfer Level (RTL) that simulate and synthesize correctly, with a focus on proper coding styles and best practices. SystemVerilog is the latest generation of the original Verilog language, and adds many important capabilities to efficiently and more accurately model increasingly complex designs. The live, instructor-led program comes with insightful lectures and demos. The emphasis is on reviewing new data types, structs, arrays, procedural blocks, enhanced procedural constructs, reusable tasks, functions and packages. The course focuses on targeting and optimizing Xilinx devices using SystemVerilog.

Who can attend?
- Undergraduate students in III or Final year of Engineering
- Post graduate students interested in brushing up their skills in Verilog
- Working professionals interested in up-skilling
- FPGA designers and Logic designers
- RTL design engineers

Pre-requisites:
- Knowledge of digital circuits
- Basic HDL Knowledge (Verilog or VHDL)

Course duration:
- 3 days (9 hours – 3 hours per day)

What do I gain?
- Describe the benefits and features of SystemVerilog for RTL design
- Identify the new data types supported in SystemVerilog
- Use an enumerated data type for coding a FSM
- Explain how to use arrays, structures and unions for RTL coding
- Describe the new procedural blocks and their effect on Synthesis
- Define the ability to reuse tasks, functions and packages
- Identify how to simplify module definitions and module instantiations using interfaces
- Target and optimize Xilinx devices using SystemVerilog
- Synthesize and Simulate SystemVerilog designs with the Vivado Design Suite

Course Contents:
Day 1
- Introduction to SystemVerilog HDVL- SV data types and operators- Two state and Four state data types – Logic vs Reg – Byte vs bit – Integer vs int
- Lab 1: SV Data types
Review of Verilog positional and named associations - SystemVerilog Implicit .name and Implicit .* associations
Simulation and Synthesis Guidelines – Case study
Lab 2: SV Associations

Day 2
- Lab 1: SV Procedural blocks and Procedural constructs
- Introduction to Enumerated Data types – Built in methods - Modeling FSM using Enum-Parameters Vs Enum
- Lab 2: FSM Modeling using SV enumerated data types
- SystemVerilog Aggregate data types – Arrays, Structures and Unions- Packed and Unpacked arrays- Packed Structures and Packed unions
- Lab 3: SV Structures and Unions

Day 3:
- Review of Verilog tasks and functions – SV reusable tasks and functions – Functions with void and return – Enhancements to tasks
- Lab 1: SV tasks and functions
- Introduction to Packages and Typecasting, Typedef and string handling functions – Synthesis guidelines
- Lab 2: ALU modeling using SV package
- Introduction to SV Interfaces – Module instantiations and definitions with and without interfaces – Advantages of Interfaces
- Lab 3: SV Interface
- Design optimization – Xilinx Specific Implementations

Course Fee: 3 days (9 Hours) – INR 1,999/- (Non-refundable, Inclusive of tax)

Last date for confirmation: 20-Dec-2020

Registration link: Click here to register

Payment Guidelines:
Participants of Sandeepani training modules can make the course fee payment through online transfer via your Internet Banking Account to the following account and proof of the same to be scanned & mailed to xtc@coreel.com.

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