Professional Development Course on VLSI – SoC Functional Verification using SystemVerilog and UVM (Full-time)

Sandeepani offers the Professional Development Course for recent graduates and post-graduates in Electronics/Electrical/Telecommunication engineering. This program is specifically designed with an objective to provide a sound platform for the students and prepare them for a successful career in the fields of ASIC and FPGA Functional Verification.

The PDC offers the right blend of classroom teaching, quality hands-on training from 'concept-to-project', covering design methodology using industry standard tools and practices. The course includes a project work as well.

Placement assistance is provided to those who complete all modules of this course and a pre-placement test.

Course Duration: 20 Weeks		Course Structure and Outline
Mod.	Module Title	What You Learn
P1	Orientation	• Linux operating system – file system, commands • Python scripting
P2	Advanced Digital System Design	• Number systems • Logic gates • Boolean expressions • Introduction to registers and counters • Synchronous Finite State Machine Design • Data-path elements - Arithmetic Structures • Introduction to Programmable Platforms • Design Capture and Simulation • Practical Digital System Design Examples
P3	Verilog	• Hardware Modeling Overview • Verilog language concepts • Modules and Ports • Operators , Dataflow Modeling • Introduction to Test benches • Procedural Statements • Coding for Finite State Machines • Coding For Synthesis • Tasks and Functions • Advanced Verilog Test benches
P4	FPGA Design and Debugging	• FPGA Architecture - Basic Components of FPGA (LUT, CLB, Switch Matrix, IOB), FPGA Architecture of different families: 7-series and UltraScale devices, Zynq • FPGA Design Flow – Xilinx Vivado tool Flow, Reading Reports, Implementing IP cores, Debugging Using Vivado Analyzer • Optimal FPGA Design – HDL Coding Techniques for FPGA, FPGA Design Techniques, Synthesis Techniques, Implementation Options • Static Timing Analysis – Global Timing Constraints, Path specific timing constraints, Achieving Timing Closure, Introduction to Reset techniques, Clock Domain

		Crossing, Multiple Clock Domains
C1	Functional Verification with SystemVerilog	• Introduction to SystemVerilog, Programming Language Features, Bus-Functional Modeling, Basic Data Types, Interfaces • RTL Process, RTL Types • SystemVerilog Assertions, Properties, Assertions and Sequences • Clocking Blocks, Randomization, Coverage, Arrays and Queues, The Direct Programming Interface • Classes for Transactions, Class Members and Copying, Virtual Interfaces, Extending Classes for Stimulus • TLM and Channels, Component Hierarchy, Monitors and Checkers • Functional Coverage, Processes and Events
C2	UVM	• Introduction to UVM, Getting started with UVM • Monitors and Reporting • Transaction-Level Modeling • Checkers and Scoreboards • Functional Coverage • Random Stimulus Generation • Factory and Configuration • Agent Architecture • Objections, Sequences, Layered Sequences and Agents • Advanced Sequencer Topics • UVM Register Layer • AMBA APB/AHB/AXI Verification using SV and UVM
Integrated in the course	Course Project	Design/Implementation/Verification

Note:

1) The contents listed above is a representative outline and is subject to change at short notice in compliance with the current industry demands
2) Legend: P# - Primer Module, C# - Core Module