Professional Development Course on VLSI - High Performance FPGA design and debugging techniques (Full-time)

Sandeepani offers the Professional Development Course for recent graduates and post-graduates in Electronics/Electrical/Telecommunication engineering. This program is specifically designed with an objective to provide a sound platform for the students and prepare them for a successful career in the field of FPGA Design.

The PDC offers the right blend of classroom teaching, quality hands-on training from 'concept-to-project', covering design methodology using industry standard tools and practices. The course includes a project work as well.

Placement assistance is provided to those who complete all modules of this course and a pre-placement test.

<table>
<thead>
<tr>
<th>Course Duration: 16 Weeks</th>
<th>Course Structure and Outline</th>
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<tbody>
<tr>
<td>Mod.</td>
<td>Module Title</td>
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| P1 | Orientation | • Linux operating system – file system, commands  
• Python scripting |
| P2 | Advanced Digital System Design | • Number systems  
• Logic gates  
• Boolean expressions  
• Introduction to registers and counters  
• Synchronous Finite State Machine Design  
• Data-path elements - Arithmetic Structures  
• Introduction to Programmable Platforms  
• Design Capture and Simulation  
• Practical Digital System Design Examples |
| P3 | Verilog | • Hardware Modeling Overview  
• Verilog language concepts  
• Modules and Ports  
• Operators, Dataflow Modeling  
• Introduction to Test benches  
• Procedural Statements  
• Coding for Finite State Machines  
• Coding For Synthesis  
• Tasks and Functions  
• Advanced Verilog Test benches |
| P4 | FPGA Design and Debugging | • FPGA Architecture - Basic Components of FPGA (LUT, CLB, Switch Matrix, IOB), FPGA Architecture of different families: 7-series and UltraScale devices, Zynq  
• FPGA Design Flow – Xilinx Vivado tool Flow, Reading Reports, Implementing IP cores, Debugging Using Vivado Analyzer  
• Optimal FPGA Design – HDL Coding Techniques for FPGA, FPGA Design Techniques, Synthesis Techniques, Implementation Options  
• Static Timing Analysis – Global Timing Constraints, Path specific timing constraints, Achieving Timing Closure, Introduction to Reset techniques, Clock Domain |
### Crossing, Multiple Clock Domains

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<tr>
<th>Integrated in the course</th>
<th>Course Project</th>
<th>Design/Implementation</th>
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**Note:**

1) The contents listed above is a representative outline and is subject to change at short notice in compliance with the current industry demands.

2) Legend: P# - Primer Module, C# - Core Module