Online On-demand – FPGA Design Flow using Vivado

Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for AMD-Xilinx in India

Course Description:
This self-paced online course gives participants an in-depth walk-through of the FPGA Design tool flow using Vivado from AMD-Xilinx. It covers the tool flow from Design entry to Bitstream generation, Coding techniques for effective implementation, the IP Integrator and Packager, FPGA Debugging and Non-project or Batch mode of operation in Vivado. The program comes with insightful theory lectures, lab code and lab demos.

Who can attend?
- Hardware Engineers who are new to FPGA Design and Vivado
- Faculty, Research Scholars and students who need to use Vivado for their research or project work

Pre-requisites:
- Knowledge of digital circuits
- Basic HDL Knowledge (Verilog or VHDL)

Access:
- Login and password will be shared within 1 business day after payment and registration
- Content will be made available for 1 month from start of access

Software Tools:
- Xilinx Vivado

What do I gain?
- Understand the FPGA Design cycle
- Get to know the Vivado interface and features for FPGA Design
- Learn how Vivado is used for integrating IPs and on-chip debugging

Course Contents:
- Chapter 1 – FPGA Introduction
  - Video lecture – FPGA Introduction
  - Video lecture – FPGA and ASIC Flow
  - Lab demo – FPGA Design Flow using Vivado and board implementation
- Chapter 2 – Introduction to Coding Techniques
  - Video lecture – Introduction to Coding Techniques
  - Video lecture – Reset Methodology
  - Lab demo – HDL Coding Techniques
- Chapter 3 – IP Integrator and Packager
  - Video lecture – Designing with IP Integrator
  - Video lecture – Creating a Custom IP
  - Lab demo – Creating and Packaging Custom IP lab
- Chapter 4 – Debug Core
  - Video lecture – VIO and ILA
  - Lab demo – Using VIO and ILA for hardware debugging
- Chapter 5 – TCL Scripting for Vivado flow

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- Video lecture – Project and Non-project flow in Vivado
- Lab demo – Non-project batch mode in Vivado

Demo video: https://sandeepani-training.com/elearn/lesson/fpga-introduction

Course Fee: INR 4,999/- (Inclusive of tax. Course fee is non-refundable)

Registration link: Click here to register

Payment Guidelines:
Participants of Sandeepani training modules can make the course fee payment through online transfer via Google Pay/PhonePe/UPI using the below details and proof of the same to be scanned & mailed to training@coreel.com. For assistance, contact us: +91-9844182555, +91-9686690000.

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Current Account No: 0947000104207601
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