Static Timing Analysis (STA) and Clock Domain Crossing (CDC)

Sandeepani is the training division of CoreEL Technologies (I) Pvt Ltd and Authorized Training Provider for AMD in India

Dates: 12th Jun – 14th Jun 2024 (Live Online sessions – 10am to 1pm)

Course Description:
This live, online course helps to review the underlying database and static timing analysis (STA) mechanisms. The live, instructor-led program comes with insightful lectures and demos. The emphasis is on utilizing project based scripting flow for navigating the design, creating Xilinx design constraints and analyzing timing reports. The course focuses on creating path specific constraints, false paths, max and min delay constraints and priority of the timing exceptions in the Vivado timing engine. The course also addresses on various synthesis and implementation techniques for achieving better timing closure.

Highlights:
**** Cloud-based Vivado tool access**

Who can attend?
- FPGA Engineers interested in understanding how to constrain designs for timing
- Digital Design engineers interesting in learning about Static Timing Analysis for their designs

Pre-requisites:
- Knowledge of digital circuits
- Basic HDL Knowledge (Verilog or VHDL)

Course duration:
- 3 days (9 hours – 3 hours per day)

What do I gain?
- Describe setup and hold checks
- Create appropriate clock, input and output delay XDC constraints
- Timing Exceptions
- Analyze different timing reports
- Define a properly constrained design
- Identify key areas to optimize the design to meet performance goals and objectives
- Clock Domain Crossing
- Analyze Clock Domain Crossing Reports
- Synthesis Techniques- Pipelining, Register duplication and Retiming
- Implementation Techniques- Physical optimization and Floor-planning

Course Contents:
Day 1
- Introduction to Static Timing Analysis
- Static Timing Analysis - Setup and Hold check (Equations)
- Timing Paths - Reg to Reg path, Input to Reg path, Reg to Output paths
- Introduction to Xilinx Design Constraints
- Clock Variations and Uncertainties
- Baselining Flow - Clock Constraints, I/O constraints and Virtual clocks, Timing Exceptions
- Lab 1: Baselining Flow – Applying Multiple Clock Constraints for different practical scenarios
- Lab 2: Baselining Flow – Applying I/O Constraints and Virtual Clocks
- Lab 3: Baselining Flow – Understanding Timing Exceptions and analyzing timing reports

Day 2:

- Reducing Logic and Net Delay
- Improving Clock Skew and Clock Uncertainty
- Synchronization Techniques – Addressing Metastability issues using Single Bit Metastability Resolution Circuits and Asynchronous FIFOs.
- Understanding the requirement of Reset Bridge
- Constraining and reporting CDC for Resolution Circuits
- Lab 1: Improving Clock Uncertainty – Applying the parallel BUFGCE_DIV technique
- Lab 2: CDC Case Study – Generate CDC report and apply ASYNG_REG property in your design
- Lab 3: CDC Case Study – Working with Asynchronous FIFO IP for multibit CDC

Day 3:

- Synthesis Techniques – Pipelining, Retiming, Resource Sharing and Register duplication
- Congestion Analysis and Reduction Techniques
- Implementation techniques – Physical optimization, Floor Planning
- AMD-Xilinx Design Methodology for Timing Closure Techniques
- Lab 1: Synthesis Techniques – Applying Pipelining for improving performance of design
- Lab 2: Physical Optimization – Understand the Physical Optimization technique used for Timing Closure
- Lab 3: Floor Planning – Floorplan a complex design using Pblocks

Course Fee: INR 6,500/- (Inclusive of tax, non-refundable)

Last date for confirmation: 11th Jun 2024

Registration link: Click here to register

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