Online Internship on Xilinx SoC Design Flow

(Live Online sessions – 1 hour/day, Mon to Fri)

Description:
Sandeepani offers 1 month Online Internship Program for students currently doing their B.E/B.Tech, M.E./M.Tech in Electronics/ Instrumentation/Electrical/ Telecommunication. This program is specifically designed with an objective to spark an interest in Digital System Design and Embedded System Design using Xilinx tools. The participants will get an opportunity to work on a project during the course.

Highlights:
**** Cloud-based FPGA board access**
**** Training for Interview Preparation**
**** Opportunity to work on a project**

Key takeaways:
- Introduction to Digital VLSI design flow – ASIC/FPGA/SoC Design Flow
- Verilog HDL language constructs
- Modelling Digital Circuits using Verilog HDL
- Functional simulation – Verilog Test Benches
- Coding For Synthesis, Verilog HDL coding Guidelines
- FPGA Design Flow – Xilinx Vivado tool Flow, RTL Analysis, Synthesis, Implementation, Bitstream Generation, Hardware Implementation on remote FPGA board
- Introduction to Zynq SoC Architecture
- Embedded System Design Flow using Xilinx Vitis
- Extend the hardware system with Xilinx provided peripherals

Eligibility criteria:
- Pursuing UG/PG/Research, Graduate/Post Graduate Student, Faculty, Working professional

Tools/Hardware/Software:
- Vivado, Vitis, Zynq-7000 SoC board

Key topics covered:
Week 1
- Introduction to Digital Electronics
- Combinational Logic – Logic gates, arithmetic circuits, code converters, multiplexers, decoders / encoders
- Sequential circuits – latches and flip-flops, counters, shift-registers and finite state machines
- Introduction to Digital VLSI design flow – ASIC/FPGA/SoC Design Flow
- Introduction to Verilog HDL - Levels of Abstraction, Verilog HDL language constructs - Keywords, Identifiers, Comments, Verilog Data types, Verilog Modelling Styles, Verilog Operators, Synthesizable and Non-Synthesizable Verilog constructs
- Introduction to Data flow modelling – Continuous Assignment – Combinational Logic – Modelling Adders, Muxs, Decoder/ Encoder logic

Week 2
- Introduction to Data flow modelling – Continuous Assignment – Sequential Logic – Modelling D Latch / T Latch, D FF / T FF Master Slave Configuration
- Introduction to Structural modelling – Module Instantiation – Gate Level Design, Hierarchical design – Modelling Ripple carry adder, Carry look ahead adder, Multipliers

- Introduction to Behavioural modelling – Procedural Assignment – Procedural Assignment vs Continuous Assignment, Rules for Procedural Block, Always Block and Initial Block, Conditional statements and Looping statements

Week 3

- Introduction to Functional Simulation – Testbench Architecture – Writing Test Bench in Verilog HDL – Test Bench for Combinational and Sequential Logic
- Finite State Machine – Moore and Mealy FSM – FSM Coding Techniques
- HDL Coding Guidelines
- Simulation-Synthesis mismatch
- Mini-project

Week 4

- Introduction to FPGA Design Flow, ASIC vs FPGA Design Flow, Xilinx FPGA 7 Families
- Vivado Design Suite tool flow
- Demo on Verilog Code to Bitstream generation and FPGA implementation
- Introduction to Zynq-7000 SoC
- Vitis tool flow
- Creating a Simple Embedded Hardware Design
- Extending Hardware System by Adding Peripherals

Week 5

- Project implementation on FPGA board

Course Fee: 1 month (1 hour/day) – INR 10,000/- (Inclusive of tax, Non-refundable)

Registration link: Click here to register

For more details, contact Swathi: +91-9686690000